

CP series CP1H CPU Unit CP1H-X DD - CP1H-Y DD - CP1H-XA D

4 Axis Position Control and Comprehensive Programmable Controller

- The CP1H-X with pulse outputs for 4 axes.
- The CP1H-Y with 1-MHz pulse I/O.
- The CP1H-XA with pulse outputs for 4 axes and built-in analog I/O.



Features

- Pulse output for 4 axes. Advanced power for high-precision positioning control.
- High-speed counters. Differential phases for 4 axes. Easily handles multi-axis control with a single unit.
- Eight interrupt inputs are built in. Faster processing of approximately 500 instructions speeds up the entire system.
- Serial communications. Two ports. Select Option Boards for either RS-232C or RS-485 communications.
- Ethernet Communications. Enabled by using an Option Board. Two ports can be used as an Ethernet port to perform. Ethernet communications between the CP1H and a host computer.
- Built-in Analog I/O. XA CPU Units provide 4 input words and 2 output words.
- USB Peripheral Port. Another standard feature.
- The structured text (ST) language. Makes math operations even easier.
- Can be used for the CP1W series and CJ series Unit. The extendibility of it is preeminently good.
- LCD displays and settings. Enabled using Option Board.

| Category | Name | Specifications | | Model | | | | | | |
|----------------------|-----------------------|---|--|---------------|--|--|--|--|--|--|
| | Controller Link Units | Wired (shielded twisted-pair cable) | | CJ1W-CLK23 | | | | | | |
| | | 1 RS-232C port and 1 RS-422A/485 port | | CJ1W-SCU42 | | | | | | |
| | | 2 RS-232C ports | | CJ1W-SCU22 | | | | | | |
| | Serial Communications | 2 RS-422A/485 ports | | CJ1W-SCU32 | | | | | | |
| | Units | 1 RS-232C port and 1 RS-422A/485 port | | CJ1W-SCU41-V1 | | | | | | |
| | | 2 RS-232C ports | | CJ1W-SCU21-V1 | | | | | | |
| | | 2 RS-422A/485 ports | | CJ1W-SCU31-V1 | | | | | | |
| CJ1 CPU Bus Units | EtherNet/IP Unit | Shielded twisted-pair cable (STP), category 5 or 5e or I Tag data links and message communications supporte | lded twisted-pair cable (STP), category 5 or 5e or higher data links and message communications supported | | | | | | | |
| bus offics | Ethernet Unit | 100Base-TX | | CJ1W-ETN21 | | | | | | |
| | DeviceNet™ Unit | Functions as master and/or slave; allows control of 32, | 000 points max. per master | CJ1W-DRM21 | | | | | | |
| | | Control common de controlie y MECHATROLINIK II | 2 axes | CJ1W-NC271 | | | | | | |
| | MECHATROLINK-II | Control commands sent using MECHATROLINK-II synchronized communications | 4 axes | CJ1W-NC471 | | | | | | |
| | Position Control Unit | 16 axes max., direct operation from ladder diagram, control modes: position/ speed/torque | 16 axes | CJ1W-NCF71 | | | | | | |
| | | control modes, position/ speed/torque | 16 axes | CJ1W-NCF71-MA | | | | | | |
| | FI-net Unit | | CJ1W-FLN22 | | | | | | | |
| | SPU | High-speed Data Storage Unit | CJ1W-SPU01-V2 | | | | | | | |

Note: Refer to the CJ1 catalog (Cat. No. P052) for information on the CJ1 CPU Bus Units.

■ Industrial Switching Hubs

| | | Specifications | 3 | | | Current | |
|----------------|------------|--|--------------|-------------------|--|-----------------|----------|
| Product name | Appearance | Functions | No. of ports | Failure detection | Accesories | consumption (A) | Model |
| Industrial | 1000 | Quality of Service (QoS): EtherNet/IP TM control data priority - Failure detection: | 3 | No | Power supply connector | 0.22 | W4S1-03B |
| Switching Hubs | _ | Broadcast storm and LSI error | 5 | No | | 0.22 | W4S1-05B |
| Ownership Hubs | | detection 10/100BASE-TX, Auto- Negotiation | 5 | Yes | Power supply connector Connector for informing error | 0.22 | W4S1-05C |

General Specifications

| Туре | AC power supply models | DC power supply models | | | | | | |
|------------------------------------|--|---|--|--|--|--|--|--|
| Item Model | CP1H-□□□-A | CP1H-□□□-D | | | | | | |
| Power supply | 100 to 240 VAC 50/60 Hz | 24 VDC | | | | | | |
| Operating voltage range | 85 264 VAC | 20.4 to 26.4 VDC (with 4 or more Expansion Units and Expansion I/O Units: 21.6 to 26.4 VDC) | | | | | | |
| Power consumption | 100 VA max. (CP1H-□□□-A)(page 28) | 50 W max. (CP1H-□□□-D)(page 28) | | | | | | |
| Inrush current (See note.) | 100 to 120 VAC inputs: 20 A max. (for cold start at room temperature) 8 ms max. 200 to 240 VAC inputs: 40 A max. (for cold start at room temperature), 8 ms max. | 30 A max. (for cold start at room temperature) 20 ms max. | | | | | | |
| External power supply | 300 mA at 24 VDC | None | | | | | | |
| Insulation resistance | $20~\text{M}\Omega$ min. (at 500 VDC) between the external AC terminals and GR terminals | No insulation between primary and secondary for DC power supply | | | | | | |
| Dielectric strength | 2,300 VAC at 50/60 Hz for 1 min between the external AC and GR terminals, leakage current: 5 mA max. | No insulation between primary and secondary for DC power supply | | | | | | |
| Noise immunity | Conforms to IEC 61000-4-4. 2 kV (power supply line) | | | | | | | |
| Vibration resistance | Conforms to JIS C60068-2-6. 10 to 57 Hz, 0.075-mm amplitude, 80 minutes each. Sweep time: 8 minutes \times 10 sweeps = total tim | | | | | | | |
| Shock resistance | Conforms to JIS C60068-2-27. 147 m/s2 three times each in X, Y | ', and Z directions | | | | | | |
| Ambient operating temperature | 0 to 55°C | | | | | | | |
| Ambient humidity | 10% to 90% (with no condensation) | | | | | | | |
| Ambient operating environ- ment | No corrosive gas | | | | | | | |
| Ambient storage temperature | –20 to 75°C (Excluding battery.) | | | | | | | |
| Power holding time | 10 ms min. | 2 ms min. | | | | | | |

Note: The above values are for a cold start at room temperature for an AC power supply, and for a cold start for a DC power supply.

- A thermistor (with low-temperature current suppression characteristics) is used in the inrush current control circuitry for the AC power supply. The thermistor will not be sufficiently cooled if the ambient temperature is high or if a hot start is performed when the power supply has been OFF for only a short time. In those cases the inrush current values may be higher (as much as two times higher) than those shown above. Always allow for this when selecting fuses and breakers for external circuits.
- A capacitor charge-type delay circuit is used in the inrush current control circuitry for the DC power supply. The capacitor will not be charged if a hot start is performed when the power supply has been OFF for only a short time, so in those cases the inrush current values may be higher (as much as two times higher) than those shown above.

CP1H

Performance Specifications

| | Туре | CP1H-XA CPU Units | CP1H-X CPU Units | CP1H-Y CPU Units | | | | | | | | | |
|----------------------------|--------------------------------|--|---|--|--|--|--|--|--|--|--|--|--|
| Item | Models | CP1H-XA | CP1H-X | CP1H-Y | | | | | | | | | |
| Control met | | Stored program method | | tallallar tal | | | | | | | | | |
| I/O control r | nethod | Cyclic scan with immediate refresh | ing | | | | | | | | | | |
| Program lar | guage | Ladder diagram | | | | | | | | | | | |
| Function blo | neke | Maximum number of function block | definitions: 128 Maximum number | of instances: 256 | | | | | | | | | |
| runction bit | JCKS | Languages usable in function block | definitions: Ladder diagrams, struc | etured text (ST) | | | | | | | | | |
| Instruction | | 1 to 7 steps per instruction | | | | | | | | | | | |
| Instructions | | Approx. 500 (function codes: 3 digi | · | | | | | | | | | | |
| | execution time | Basic instructions: 0.10 μs min. Sp | ecial instructions: 0.15 μs min. | | | | | | | | | | |
| | ocessing time | 0.7 ms | | | | | | | | | | | |
| Program ca | | 20K steps | | | | | | | | | | | |
| Number of t | asks Scheduled | 288 (32 cyclic tasks and 256 interru | ıpt tasks) | | | | | | | | | | |
| | interrupt tasks | 1 (interrupt task No. 2, fixed) | | | | | | | | | | | |
| | Input interrupt | 8 (interrupt task No. 140 to 147, fixe | ed) | 6 (interrupt task No. 140 to 145, fixed) | | | | | | | | | |
| | tasks | · ' | ed and executed for high-speed cou | | | | | | | | | | |
| Maximum sı | ubroutine number | 256 | | | | | | | | | | | |
| | mp number | 256 | | | | | | | | | | | |
| | Input bits | 272bits (17 words) : CIO 0.00 to 16 | .15 | | | | | | | | | | |
| | Output bits | 272bits (17 words) : CIO 100.00 to | | | | | | | | | | | |
| I/O areas | Built-in Analog | CIO 200 to CIO 203 | | | | | | | | | | | |
| (See note.) | Inputs Built-in Analog Outputs | CIO 210 to CIO 211 | | ••• | | | | | | | | | |
| | Serial PLC Link Area | 1,440 bits (90 words): CIO 3100.00 | to CIO 3189.15 (CIO 3100 to CIO | 3189) | | | | | | | | | |
| Work bits | | 8,192 bits (512 words): W0.00 to W CIO Area: 37,504 bits (2,344 words | /511.15 (W0 to W511) s): CIO 3800.00 to CIO 6143.15 (CIO | O 3800 to CIO 6143) | | | | | | | | | |
| TR Area | | 16 bits: TR0 to TR15 | , | , | | | | | | | | | |
| Holding Are | a | 8,192 bits (512 words): H0.00 to H5 | 511.15 (H0 to H511) | | | | | | | | | | |
| AR Area | | Read-only (Write-prohibited): 7168 | Read-only (Write-prohibited): 7168 bits (448 words): A0.00 to A447.15 (A0 to A447) | | | | | | | | | | |
| An Alea | | Read/Write: 8192 bits (512 words): A448.00 to A959.15 (A448 to A959) | | | | | | | | | | | |
| Timers | | 4,096 bits: T0 to T4095 | | | | | | | | | | | |
| Counters | | 4,096 bits: C0 to C4095 | | | | | | | | | | | |
| DM Area | | 32 Kwords: D0 to D32767 | | | | | | | | | | | |
| Data Regist | | 16 registers (16 bits): DR0 to DR15 | i | | | | | | | | | | |
| Index Regis | | 16 registers (32 bits): IR0 to IR15 | | | | | | | | | | | |
| Task Flag A | | 32 flags (32 bits): TK0000 to TK003 | | | | | | | | | | | |
| Trace Memo | ory | | race data maximum of 31 bits and 6 | S words.) | | | | | | | | | |
| Memory Cas | ssette | A special Memory Cassette (CP1W Note: Can be used for program bac | kups and auto-booting. | | | | | | | | | | |
| Clock functi | on | -2.0 min to +2.0 min (ambient temp | ation): -4.5 min to -0.5 min (ambie perature: 25°C), -2.5 min to +1.5 m | in (ambient temperature: 0°C) | | | | | | | | | |
| | | | 1): For connecting Support Softwar | • | | | | | | | | | |
| Communica | tions functions | | cations Option Boards can be mou | | | | | | | | | | |
| | | A maximum of two Ethernet Option mounted. | Boards can be mounted. When using | ng CP1W-CIF41 Ver.1.0, one Ethernet Option Board can be | | | | | | | | | |
| Memory bac | kup | Flash memory: User programs, parameters (such as the PLC Setup), comment data, and the entire DM Area can be saved to flash memory as initial values. Battery backup: The Holding Area, DM Area, and counter values (flags, PV) are backed up by a battery. | | | | | | | | | | | |
| Battery serv | rice life | 5 years at 25°C. (Use the replacement battery within two years of manufacture,) | | | | | | | | | | | |
| Dattery Serv | ice ine | 20 (12 inputs, 8 outputs) | | | | | | | | | | | |
| Built-in inpu | t terminals | 40 (24 inputs, 16 outputs) | | Line-driver inputs: Two axes for phases A, B, and Z Line-driver outputs: Two axes for CW and CCW | | | | | | | | | |
| Number of o Expansion (| onnectable I/O) Units | , | J-series Special I/O Units or CPU B | us Units: 2 max. | | | | | | | | | |
| Max. numbe | r of I/O points | 320 (40 built in + 40 per Expansion | (I/O) Unit × 7 Units) | 300 (20 built in + 40 per Expansion (I/O) Unit × 7 Units) | | | | | | | | | |
| Interrupt inp | outs | 8 inputs (Shared by the external int the quick-response inputs.) | external interrupt inputs (counter mode) and 6 inputs (Shared by the external interrupts.) 6 inputs (Shared by the external interrupts.) | | | | | | | | | | |
| Interrupt inp | out counter mode | 8 inputs (Response frequency: 5 kt 16 bits Up or down counters | Hz max. for all interrupt inputs), | 6 inputs (Response frequency: 5 kHz max, for all interrupt inputs), 16 bits Up or down counters | | | | | | | | | |
| Quick-respo | nse inputs | 8 points (Min, input pulse width: 50 μs max.) 6 points (Min, input pulse width: 50 μs max.) | | | | | | | | | | | |
| Scheduled i | nterrupts | 1 | | | | | | | | | | | |
| | | | | | | | | | | | | | |

| | Туре | CP1H-XA CPU Units | CP1H-X CPU Units | CP1H-Y CPU Units | | | | | | |
|--|--------------------|---|---------------------------------|--|--|--|--|--|--|--|
| Item | Models | CP1H-XA□□□-□ | CP1H-X | CP1H-Y | | | | | | |
| High-speed cour | nters | 100 kHz Value range: 32 bits, Line | direction, up/down, increment), | 2 inputs: Differential phases (4x), 500 kHz or Single-phase, 1 MHz and 2 inputs: Differential phases (4x), 50 kHz or Single-phase (pulse plus direction, up/down, increment), 100 kHz Value range: 32 bits, Linear mode or ring mode Interrupts: Target value comparison or range comparison | | | | | | |
| Pulse outputs (models with transistor out- puts only) | Pulse out- puts | Trapezoidal or S-curve acceleration (Duty ratio: 50% fixed) 4 outputs, 1 Hz to 100 kHz (CCW/6 | | Trapezoidal or S-curve acceleration and deceleration (Duty ratio: 50% fixed) 2 outputs, 1 Hz to 1 MHz (CCW/CW or pulse plus direction) 2 outputs, 1 Hz to 100 kHz (CCW/CW or pulse plus direction) | | | | | | |
| | PWM out- puts | Duty ratio: 0.0% to 100.0% (Unit: 0 2 outputs, 0.1 to 6553.5 Hz (Accura | | | | | | | | |
| Built-in analog I/ | O terminals | 4 analog inputs and 2 analog outputs | None | | | | | | | |
| Analog control | | 1 (Setting range: 0 to 255) | | | | | | | | |
| External analog | input | 1 input (Resolution: 1/256, Input range: 0 to 10 V), not isolated | | | | | | | | |

Note: The memory areas for CJ-series Special I/O Units and CPU Bus Units are allocated at the same as for the CJ-series. For details, refer to the CJ Series catalog (Cat. No. P052).

Built-in Inputs / Built-in Outputs

■ Terminal Block Arrangement

● CP1H-XA and X CPU Units with AC Power Supply

| | | ICIO 0 | | | | | | | ICIC | 1 | | | | | | | |
|---|-----------|--------|-----|------|------|----|----|-----|------|----|-----|-----|-----|----|----|----|---------------------|
| Γ | L1 → L2/N | COM | 01 | 03 | 05 | 07 | 09 | - 1 | 1 C | 1 | 03 | 0.5 | . 0 | 7 | 09 | 11 | (Input |
| Ŀ | • 🛊 (| 9 (| 0 (| 12 (|)4 (|)6 | 08 | 10 | 00 | 02 | 2 (| 04 | 06 | 08 | | 0 | termina l s) |

| 1 | - | - | 00 | (| 01 | | 12 | 03 | | 04 | 06 | Т | 00 | 0 | 11 | 0: | 3 | C | 14 | 01 | 6 | • | (Output |
|---|---|---|----|---|----|---|-----|-----|---|----|----|----|-----|----|----|----|----|---|----|----|---|---|---------------------|
| I | • | _ | CC | M | 00 | M | CON | 1 C | M | 08 | 5 | 07 | OC. | MC | 0: | 2 | 00 | М | 0 | 5 | 0 | 7 | termina l s) |

● CP1H-XA and X CPU Units with DC Power supply

| | | | CIO | 0 | | | | | | | | | | CIO | 1 | | | | | | | | | | | |
|---|----|---|-----|---|----|----|----|-----|----|----|----|----|---|-----|---|----|---|----|---|----|---|----|---|----|---|------------|
| + | 4⊦ | - | CC | M | 01 | 0: | 3 | 05 | 07 | Т | 09 | 1 | 1 | 0 | 1 | 03 | П | 05 | П | 07 | П | 09 | , | 11 | 1 | (Input |
| • | NC | (| € | С | 10 | 02 | 04 | . (|)6 | 08 | | 10 | C | 10 | 0 | 2 | 0 | 4 | 0 | 6 | 0 | 8 | 1 | 0 | • | terminals) |
| | | | | | | | | | | | | | | | | | | | | | | | | | | |

| | N | С | О | 10 | С | 11 | 0 | 12 | 0 | 3 | 0 | 14 | (| 16 | С | 0 | 0 | 11 | (|)3 | С |)4 | (| 16 | • | (Output |
|---|---|----|---|----|---|----|---|----|---|----|---|----|---|----|---|----|---|----|---|----|---|----|---|----|---|------------|
| • | · | NO | 3 | CC | М | CO | M | CO | V | CO | М | 08 | ō | 07 | | CC | | 0: | 2 | CC | M | 06 | 5 | 0 | 7 | terminals) |

■ Built-in Input Area

● CP1H-XA and X CPU Units

| PLC Se | etup | | Input operati | on | High-speed counter operation | Pulse output origin search function set to be used. |
|--------|------|-----------------|-------------------|------------------------|---|---|
| | | Normal inputs | Interrupt inputs | Quick-response inputs | High-speed counters | Origin search |
| CIO 0 | 00 | Normal input 0 | Interrupt input 0 | Quick-response input 0 | | Pulse 0: Origin input signal |
| | 01 | Normal input 1 | Interrupt input 1 | Quick-response input 1 | High-speed counter 2 (phase-Z/reset) | Pulse 0: Origin proximity input signal |
| | 02 | Normal input 2 | Interrupt input 2 | Quick-response input 2 | High-speed counter 1 (phase-Z/reset) | Pulse output 1: Origin input signal |
| | 03 | Normal input 3 | Interrupt input 3 | Quick-response input 3 | High-speed counter 0 (phase-Z/reset) | Pulse output 1: Origin proximity input signal |
| | 04 | Normal input 4 | | | High-speed counter 2 (phase-A, increment, or count input) | |
| | 05 | Normal input 5 | | | High-speed counter 2 (phase-B, decrement, or direction input) | |
| | 06 | Normal input 6 | | | High-speed counter 1 (phase-A, increment, or count input) | |
| | 07 | Normal input 7 | | | High-speed counter 1 (phase-B, decrement, or direction input) | |
| | 08 | Normal input 8 | | | High-speed counter 0 (phase-A, increment, or count input) | |
| | 09 | Normal input 9 | | | High-speed counter 0 (phase-B, decrement, or direction input) | |
| | 10 | Normal input 10 | | | High-speed counter 3 (phase-A, increment, or count input) | |
| | 11 | Normal input 11 | | | High-speed counter 3 (phase-B, decrement, or direction input) | |
| CIO 1 | 00 | Normal input 12 | Interrupt input 4 | Quick-response input 4 | High-speed counter 3 (phase-Z/reset) | Pulse output 2: Origin input signal |
| | 01 | Normal input 13 | Interrupt input 5 | Quick-response input 5 | | Pulse output 2: Origin proximity input signal |
| | 02 | Normal input 14 | Interrupt input 6 | Quick-response input 6 | | Pulse output 3: Origin input signal |
| | 03 | Normal input 15 | Interrupt input 7 | Quick-response input 7 | | Pulse output 3: Origin proximity input signal |
| | 04 | Normal input 16 | | | | |
| | 05 | Normal input 17 | | | | |
| | 06 | Normal input 18 | | | | |
| | 07 | Normal input 19 | | | | |
| | 08 | Normal input 20 | | | | |
| | 09 | Normal input 21 | | | | |
| | 10 | Normal input 22 | | | | |
| | 11 | Normal input 23 | | | | |

■ Built-in Output Area

● CP1H-XA and CP1H-X CPU Units

| | truc- ions | When the instructions to the right are not executed | | output instruction , or ORG) is executed | When the origin search function is set to be used in the PLC Setup, and an origin search is executed by the ORG instruction | When the PWM instruction is executed |
|---------|---------------|---|----------------------|---|--|--------------------------------------|
| DI C | Setup | Normal outputs | | Fixed duty ratio p | ulse outputs | Variable duty ratio pulse output |
| r L C 、 | etup | Normal outputs | CW/CCW | Pulse plus direction | When the origin search function is used | PWM output |
| CIO | 00 | Normal output 0 | Pulse output 0 (CW) | Pulse output 0 (pulse) | | |
| 100 | 01 | Normal output 1 | Pulse output 0 (CCW) | Pulse output 1 (pulse) | | |
| | 02 | Normal output 2 | Pulse output 1 (CW) | Pulse output 0 (direction) | | |
| | 03 | Normal output 3 | Pulse output 1 (CCW) | Pulse output 1 (direction) | | |
| | 04 | Normal output 4 | Pulse output 2 (CW) | Pulse output 2 (pulse) | | |
| | 05 | Normal output 5 | Pulse output 2 (CCW) | Pulse output 2 (direction) | | |
| | 06 | Normal output 6 | Pulse output 3 (CW) | Pulse output 3 (pulse) | | |
| | 07 | Normal output 7 | Pulse output 3 (CCW) | Pulse output 3 (direction) | | |
| CIO | 00 | Normal output 8 | | | | PWM output 0 |
| 101 | 01 | Normal output 9 | | | | PWM output 1 |
| | 02 | Normal output 10 | | | Origin search 0 (Error counter reset output) | |
| | 03 | Normal output 11 | | | Origin search 1 (Error counter reset output) | |
| | 04 | Normal output 12 | | | Origin search 2 (Error counter reset output) | |
| | 05 | Normal output 13 | | | Origin search 3 (Error counter reset output) | |
| CIO | 06 | Normal output 14 | | | | |
| 101 | 07 | Normal output 15 | | | | |

■ Terminal Block Arrangement

● CP1H-Y CPU Units



Note: Supply 24 VDC to the bottom 24 VDC input terminals when using bits 04 to 07 of output word CIO 100.

■ Built-in Input Area

● CP1H-Y CPU Units

| PLC S | Setup | | Input operation s | setting | High-speed counter operation setting | Pulse output origin search function set to be used. |
|-------|--------|-----------------|-------------------|------------------------|---|---|
| | | Normal inputs | Interrupt inputs | Quick-response inputs | High-speed counters | Origin search |
| А | 70 | | | | High-speed counter 0 (phase-A, increment, or count input) fixed | |
| В | 0 | | | | High-speed counter 0 (phase-B, decrement, or direction input) fixed | |
| Z | :0 | | | | High-speed counter 0 (phase-Z/reset) fixed | Pulse 0: Origin input signal (line driver) |
| А | .1 | | | | High-speed counter 1 (phase-A, increment, or count input) fixed | |
| В | 1 | | | | High-speed counter 1 (phase-B, decrement, or direction input) fixed | |
| Z | 1 | | | | High-speed counter 1 (phase-Z/reset) fixed | Pulse 1: Origin input signal (line driver) |
| CIO 0 | Bit 00 | Normal input 0 | Interrupt 0 | Quick-response input 0 | | Pulse 2: Origin proximity input signal |
| | Bit 01 | Normal input 1 | Interrupt 1 | Quick-response input 1 | High-speed counter 2 (phase-Z/reset) | |
| | Bit 04 | Normal input 2 | | | High-speed counter 2 (phase-A, increment, or count input) | |
| | Bit 05 | Normal input 3 | | | High-speed counter 2 (phase-B, decrement, or direction input) | |
| | Bit 10 | Normal input 4 | | | High-speed counter 3 (phase-A, increment, or count input) | |
| | Bit 11 | Normal input 5 | | | High-speed counter 2 (phase-B, decrement, or direction input) | Pulse 3: Origin proximity input signal |
| CIO 1 | Bit 00 | Normal input 6 | Interrupt 2 | Quick-response input 2 | High-speed counter 2 (phase-Z/reset) | Pulse 3: Origin input signal |
| | Bit 01 | Normal input 7 | Interrupt 3 | Quick-response input 3 | | Pulse 2: Origin input signal |
| | Bit 02 | Normal input 8 | Interrupt 4 | Quick-response input 4 | | Pulse 1: Origin input signal (open collector) |
| | Bit 03 | Normal input 9 | Interrupt 5 | Quick-response input 5 | | Pulse 0: Origin input signal (open collector) |
| | Bit 04 | Normal input 10 | | | | Pulse 1: Origin proximity input signal |
| | Bit 05 | Normal input 11 | | | | Pulse 0: Origin proximity input signal |

These areas are for line-driver inputs, so they can be used only for high-speed counters (1 MHz) and not for other purposes, such as normal inputs.

■ Built-in Output Area

● CP1H-Y CPU Units

| Instructions | | When the instructions to the right are not executed | | output instruction , or ORG) is executed | When the origin search function is set to be used in the PLC Setup, and an origin search is executed by the ORG instruction | When the PWM instruction is executed |
|--------------|---|---|-------------------------------|---|--|--------------------------------------|
| PLC Setup | | Normal autnut | Fixed duty ratio pulse output | | | Variable duty ratio pulse output |
| | | Normal output | CW/CCW | Pulse plus direction | When the origin search function is used | PWM output |
| C' | CW0 Not supported. Pulse output 0 (CW) Pulse output 0 (pulse) fixed | | | | | |
| CC | CCW0 Not supported. | | Pulse output 0 (CCW) fixed | Pulse output 1 (pulse) fixed | | |
| CW1 | | Not supported. | Pulse output 1 (CW) fixed | Pulse output 0 (direction) fixed | | |
| CCW1 | | Not supported. | Pulse output 1 (CCW) fixed | Pulse output 1 (direction) fixed | | |
| CIO | Bit 04 | 100.04 | Pulse output 2 (CW) | Pulse output 2 (pulse) | | |
| 100 | Bit 05 | 100.05 | Pulse output 2 (CCW) | Pulse output 2 (direction) | | |
| | Bit 06 | 100.06 | Pulse output 3 (CW) | Pulse output 3 (pulse) | | |
| | Bit 07 | 100.07 | Pulse output 3 (CCW) | Pulse output 3 (direction) | | |
| CIO | Bit 00 | 101.00 | | | Origin search 2 (Error counter reset output) | PWM output 0 |
| 101 | Bit 01 | 101.01 | | | Origin search 3 (Error counter reset output) | PWM output 1 |
| | Bit 02 | 101.02 | | | Origin search 0 (Error counter reset output) | |
| | Bit 03 | 101.03 | <u> </u> | | Origin search 1 (Error counter reset output) | |

These areas are for line-driver inputs, so they can be used only for high-speed counters (1 MHz) and not for other purposes, such as normal inputs.

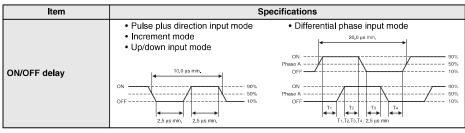
I/O Specifications for CPU Units

■ Input Specifications

| | Specifications | | | | |
|------------------------|--|--|-----------------------------|--|--|
| ITEM | High-speed counter inputs (phases A and B) | Interrupt inputs and quick-response inputs | Normal inputs | | |
| CP1H-XA/X CPU Units | CIO 0.04 to CIO 0.11 | CIO 0.00 to CIO 0.03 and CIO 1.00 to CIO 1.03 | CIO 1.04 to CIO 1.11 | | |
| CP1H-Y CPU Units | CIO 0.04, CIO 0.05, CIO 0.10, CIO 0.11 | CIO 0.00, CIO 0.01 and CIO 1.00 to CIO 1.03 | CIO 1.04, CIO 1.05 | | |
| Input voltage | 24 VDC +10%/-15% | | | | |
| Applicable sensors | 2-wire sensors or 3-wire sensors | | | | |
| Input impedance | 3.0 kΩ | 4.7 kΩ | | | |
| Input current | 7.5 mA typical | 5 mA typical | | | |
| ON voltage | 17.0 VDC min. | 14.4 VDC min. | | | |
| OFF voltage/current | 1 mA max. at 5.0 VDC | | | | |
| ON delay 2.5 μs max. | | 50 μs max. 1 ms max. | | | |
| OFF delay | 2.5 μs max. | 50 μs max. | 1 ms max. | | |
| Circuit configuration | Input LED Internal circuits | Input LED N 3,0 KO S F Internal circuits | Input LED Internal circuits | | |

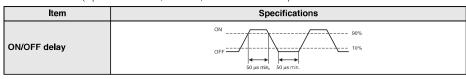
● High-speed Counter Function Input Specifications

CP1H-XA/X CPU Units (Input bits: CIO 0.04 to CIO 0.11) CP1H-Y CPU Units (Input bits: CIO 0.04, CIO 0.05, CIO 0.10, CIO 0.11)



● Interrupt Input Counter Mode

CP1H-XA/X CPU Units (Input bits: CIO 0.00 to CIO 0.03, CIO 1.00 to CIO 1.03) CP1H-Y CPU Units (Input bits: CIO 0.00, CIO 0.11, CIO 1.00 to CIO 1.03)



● High-speed Counter Inputs (Line-driver Inputs)

CP1H-Y CPU Units

| Item | Specifications | |
|--------------------------------|---|-------------------------|
| High-speed counter in- puts | Phases A and B | Phase Z |
| Input voltage | RS-422A line-driver, AM26LS31 or equivalent Note: The power supply voltage on the line-driver must be 5 V±5% max. | |
| Input type | Line-driver input | |
| Input current | 10 mA typical | 13 mA typical |
| Circuit configuration | 330 Ω 680 Ω ₹330 pF Internal circuits | 180 Ω Internal circuits |
| ON/OFF delay | Pulse plus direction input mode Increment mode Up/down input mode 1 µs min. ON OFF OFF Phase B OFF T1, T2, T3, T4: 0.5 µs min. ON T1, T2, T3, T4: 0.5 µs min. | ON Phase Z OFF |

■ Output Specifications

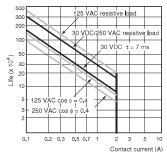
● CPU Units with Relay Outputs

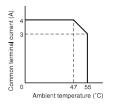
| | Item | | Specifications | |
|--------------------------|-----------------------|---------------------|--|--|
| Max. switching capacity | | | 2 A, 250 VAC (cosφ = 1), 2 A, 24 VDC 4 A/common) | |
| Min. switching capacity | | capacity | 5 VDC, 10 mA | |
| Ser- | Elec- trical | Resis- tive load | 100,000 operations (24 VDC) | |
| vice life of relay | | Induc- tive load | 48,000 operations (250 VAC, cosφ = 0.4) | |
| | Mecha | nical | 20,000,000 operations | |
| ON del | ay | | 15 ms max. | |
| OFF de | OFF delay | | 15 ms max. | |
| Circuit | Circuit configuration | | Output LED OUT | |

 $\textbf{Note:} \ \mathsf{Under} \ \mathsf{the} \ \mathsf{worst} \ \mathsf{conditions}, \ \mathsf{the} \ \mathsf{service} \ \mathsf{life} \ \mathsf{of} \ \mathsf{output} \ \mathsf{contacts} \ \mathsf{is} \ \mathsf{as} \ \mathsf{showr}$

on the left.

The service life of relays is as shown in the following diagram as a guideline.



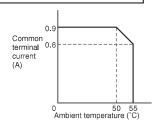


● CPU Units with Transistor Outputs (Sinking/Sourcing)

| Item | Specifications | | | | |
|-------------------------|---|--|--------------------------|--|--|
| CP1H-XA/X CPU Units | CIO 100.00 to CIO 100.07 | CIO 101.00, CIO 101.01 | CIO 101.02 to CIO 101.07 | | |
| CP1H-Y CPU Units | CIO 100.04 to CIO 100.07 | CIO 101.00, CIO 101.01 | CIO 101.02, CIO 101.03 | | |
| Max. switching capacity | 4.5 to 30 VDC: 300 mA/point, 0.9 A/common, 3.6 A/Unit *1*2 | | | | |
| Min. switching capacity | 4.5 to 30 VDC, 1 mA | | | | |
| Leakage current | 0.1 mA max. | | | | |
| Residual voltage | 0.6 V max. | 1.5 V max. | | | |
| ON delay | 0.1 ms max. | | | | |
| OFF delay | 0.1 ms max. | | 1 ms max. | | |
| Fuse | 1/common *3 | | | | |
| Circuit configuration | Sinking Outputs OUT OUT OUT OUT 4.5 to 30 VDC Sourcing Outputs COM (+) Internal circuits OUT OUT OUT 4.5 to 30 VDC OUT OUT OUT OUT 4.5 to 30 VDC | Sinking Outputs Internal circuits Sourcing Outputs | OUT | | |

Note: 1. Do not apply a voltage or connect a load to an output terminal exceeding the maximum switching capacity.

- *1 Also do not exceed 0.9 A for the total for CIO 100.00 to CIO 100.03. (CIO 100.00 to CIO 100.03 is different common.)
- *2 A maximum of 0.9 A per common can a*3 Fuses cannot be replaced by the user. A maximum of 0.9 A per common can be switched at an ambient temperature of 50 $^{\circ}\text{C}_{\bullet}$



Pulse outputs

CP1H-XA/X CPU Units: Output bits CIO 100.00 to CIO 100.07 CP1H-Y CPU Units: Output bits CIO100.04 to CIO 100.07

| Item | Specifications | |
|-------------------------|---------------------------|--|
| Max. switching capacity | 30 mA at 4.75 to 26.4 VDC | |
| Min. switching capacity | 7 mA at 4.75 to 26.4 VDC | |
| Max. output frequency | 100 kHz | |
| Output waveform | OFF 90% | |

Note: 1. The above values assume a resistive load and do not consider the impedance of the cable connecting the load.

- ${\bf 2.}\ {\bf The}\ {\bf pulse}\ {\bf widths}\ {\bf during}\ {\bf actual}\ {\bf use}\ {\bf may}\ {\bf be}\ {\bf smaller}\ {\bf than}\ {\bf the}\ {\bf ones}\ {\bf shown}$ above due to pulse distortion caused by connecting cable impedance.
- ${\bf 3.}\,$ The OFF and ON refer to the output transistor. The output transistor is ON at level "L".

Pulse Outputs (Line-driver Outputs)

CP1H-Y CPU Units

| 91 111 1 91 9 91113 | | | |
|-----------------------|---|--|--|
| Item | Specifications | | |
| Pulse outputs | Line-driver outputs, Am26LS31 or equivalent | | |
| Max. output current | 20 mA | | |
| Max. output frequency | 1 MHz | | |
| Circuit configuration | memal circuits | | |

Note: Connect a load of 20 mA or less to the output. The Unit may be damaged if a current of more than 20 mA is output.

Pulse outputs

CP1H-XA/X/Y CPU Units: Output bits CIO101.00, CIO 101.01

| Item | Specifications | |
|-------------------------|--|--|
| Max. switching capacity | 30 mA at 4.75 to 26.4 VDC | |
| Max. output frequency | 1 kHz | |
| PWM output precision | ON duty +5%, –0% at output frequency of 1 kHz | |
| Output waveform | OFF ON duty = $\frac{\text{ton}}{T} \times 100\%$ | |

Note: 1. The above values assume a resistive load and do not consider the impedance of the cable connecting the load.

- ${\bf 2.}$ The pulse widths during actual use may be smaller than the ones shown
- above due to pulse distortion caused by connecting cable impedance.

 3. The OFF and ON refer to the output transistor. The output transistor is ON at level "L".

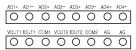
■ Analog I/O Specifications (CP1H-XA CPU Units Only)

| Item | | Voltage I/O | Current I/O | |
|----------------------------|---|---|--|--|
| | Number of analog inputs | 4 | | |
| | Input signal range | 0 to 5 V, 1 to 5 V, 0 to 10 V, or –10 to 10 V | 0 to 20 mA or 4 to 20 mA | |
| | Max. rated input | ±15 V | ±30 mA | |
| | External input impedance | 1 MΩ min. | Approx. 250 Ω | |
| Analog Input Section | Resolution | 1/6,000 or 1/12,000 (full scale) | | |
| | Overall accuracy | 25°C: ±0.3% full scale/0 to 55°C: ±0.6% full scale | 25°C: ±0.4% full scale/0 to 55°C: ±0.8% full scale | |
| | A/D conversion data | Full scale for –10 to 10 V: F448 (E890) to 0BB8 (1770) hex Full scale for other ranges: 0000 to 1770 (2EE0) hex | | |
| | Averaging | Supported (Set for individual inputs in the PLC Setup.) | | |
| | Open-circuit detection | Supported (Value when disconnected: 8000 Hex) | | |
| | Number of outputs | 2 | | |
| | Output signal range | 0 to 5 V, 1 to 5 V, 0 to 10 V, -10 to 10 V | 0 to 20 mA or 4 to 20 mA | |
| Analog | Allowable external output load resistance | 1 kΩ min. | $600~\Omega$ max. | |
| Output | External output impedance | 0.5 Ω max. | | |
| Section | Resolution | 1/6000 or 1/12000 (full scale) | | |
| | Overall accuracy | 25°C±0.4% of full scale, 0 to 55°C±0.8% of full scale | | |
| | D/A conversion data | Full scale for –10 to 10 V: F448 (E890) to 0BB8 (1770) hex Full scale for other ranges: 0000 to 1770 (2EE0) hex | | |
| Conversi | on time | 1 ms/point | | |
| Isolation | method | Photocoupler isolation between analog I/O terminals and internal circuits. No isolation between analog I/O signals. | | |

Built-in Analog Input Switch (Factory Settings)



| Built-in Analog I/O Terminal Block Arrangeme | erminal Block Arrang | ement |
|--|----------------------|-------|
|--|----------------------|-------|



External Interfaces

■ CPU Unit Nomenclature

